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13. ABSTRACT (Maximum 200 words) The purpose of this project was to determine the feasibility of developing a p-channel 2-D MESFET for future low power complementary IC technologies. The project demonstrated the fabrication of prototype p-channel 2-D MESFETs having promising electrical characteristics, developed a p-channel 2-D MESFET device model which was implemented into a commercially available SPICE program, demonstrated the SPICE simulation of p-channel 2-D MESFET device characteristics as well as complementary 2-D MESFET circuits, and demonstrated that the complementary 2-D MESFET should have significantly lower power-delay product compared with existing technologies. Finally, the project evaluated the manufacturability and technology insertion issues of the new technology.				
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**Complementary 2-D MESFET for
Low Power Electronics**

Final Report

**Air Force SBIR Phase I
Contract Number: F33615-95-C-1679**


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Complementary 2-D MESFET for Low Power Electronics (Air Force SBIR Contract F33615-95-C-1679)

Phase I Final Report

As detailed in the Phase I proposal, the project has four major tasks. These are 1) assessment of the p-channel 2-D MESFET device fabrication, 2) development of a p-channel 2-D MESFET model and implementation of the model into AIM-SPICE, 3) circuit simulations of complementary 2-D MESFET circuits using AIM-SPICE and comparison with conventional circuits, and, 4) analysis of manufacturability and technology insertion issues. This report summarizes progress in each task area during the 6 month Phase I period.

Task 1: Assessment of p-Channel Device Fabrication

On September 25, the p-channel heterostructure wafer was delivered and the p-channel 2-D MESFET fabrication began in early October at the University of Virginia (ADT employees have access to UVA facilities for a nominal fee). The fabrication of the prototype p-channel 2-D MESFETs used all optical (contact UV) lithography and standard processing techniques throughout and yielded working devices such as that shown in Fig. 1. The channel dimensions were typically L_{DS} (drain-source spacing) = W_{GG} (gate-gate spacing) = 3 μm and $L_G = 1 \mu\text{m}$. These dimensions are comparable to those in the n-channel device except for W_{GG} (the most critical dimension) which was much larger than in n-channel devices (the p-channel maskset used conservative design rules to ensure working prototype devices whereas the n-channel gates were defined using electron beam lithography).

After the Ti/Pt/Au ohmic contacts were formed, the 2-d hole gas sheet resistance of roughly $10^4 \Omega/\text{square}$ was confirmed by measuring the resistance between source and drain contacts. After device isolation (the conducting layers were etched except for the vertical bow-tie region surrounding the channel - see Fig. 1), the source-drain resistance increased by a factor of 100 to $10^6 \Omega$ (this factor is roughly equal to the ratio of the total pad perimeter divided by the final source contact width). The high series resistance therefore was attributed to high ohmic contract resistance in the prototype devices and such resistance can be easily reduced using ion implantation and by optimizing the ohmic contact technology.

The prototype p-channel 2-D MESFET I-V characteristics are shown in Fig. 2. As expected, the drain current is modulated by the lateral depletion of the 2-d hole gas as a function of gate voltage. Here, the drain current (at $V_{DS} = 8\text{V}$) varied from about 30 μA at forward gate bias down to a few microamp at reverse bias. Pinch-off was not achieved due to the large gate-gate spacing of 3 μm . The gate current is also shown and was much less than 1 μA throughout, indicating a good p-type Schottky barrier. The prototype devices had a poor turn-on characteristic (seen at low V_{DS} values in Fig. 1) which was attributed to the high ohmic contact resistance. As has been demonstrated previously in n-channel devices [3], the transistor characteristics should improve dramatically upon scaling the device width (to 1 μm and below) and upon optimization of material and processing techniques. The

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relatively large drain bias required here is also due to the high series resistance and normal FET bias range ($0 < V_{DS} < 2 \text{ V}$) will be achieved upon reduction of the series resistance.

Task 2: Development of p-Channel 2-D MESFET Model

We have developed a p-channel 2-D MESFET model based on the n-channel device model. The n-channel device model, which is described in [2], is based on the HFET models described in [1] but modified to describe the operation of the lateral gates of the 2-D MESFET. The n-channel model has been found to be in excellent agreement with measured data. The p-channel 2-D MESFET model has been implemented into AIM-Spice and is presently being used to simulate discrete p-channel 2-D MESFET I-V characteristics as well as complementary 2-D MESFET logic circuits (see below). The p-channel device model uses a lower Schottky barrier height (typically $0.55 \text{ V} - 0.6 \text{ V}$) compared with that of the n-channel device (typically 0.8 V). Also, the hole mobility has been set to $300 \text{ cm}^2/\text{Vs}$, consistent with the Hall measurements of the p-channel wafer used to fabricate prototype devices. Fig. 3 shows the I_d vs. V_{ds} and I_d vs. V_{gs} characteristics of a simulated p-channel device. This simulated device has the same current level and most of the same extracted model parameters as the prototype p-channel device; however, the series resistance values were lowered to $10 \text{ k}\Omega$ and the channel dimensions scaled to $W=L=1.0 \text{ }\mu\text{m}$. This value of series resistance should be easily achieved in future fabrication runs. Channel dimensions of $W=L=1 \text{ }\mu\text{m}$ should be easily attainable as we have fabricated n-channel devices with dimensions in the sub- $0.5 \text{ }\mu\text{m}$ range.

An important feature of both the n-channel and p-channel 2-D MESFET current-voltage model is that it describes both the above- and below-threshold regions of operation with a single analytical expression. This is especially important for circuit simulation where continuous solutions (and their derivatives) lead to better speed and convergence properties compared to other approaches. Another important feature of the model is that it is capable of simulating the dual-gate operation of the 2-D MESFET. AIM-Spice simulations of complementary 2-D MESFET (C-2DFET) inverters and ring oscillators, as well as dual-gate logic elements, are discussed in the next section.

Task 3: Complementary 2-D MESFET Circuit Simulations

The I-V and C-V AIM-Spice models for the n-channel and p-channel 2-D MESFET are being used to design low power complementary logic elements including the basic inverter and variations of a new two-input logic gate, both shown in Fig. 4. A diode was placed in series with the gate of the p-channel device to reduce gate leakage and allow the inverter to operate with supply voltages higher than 0.5 V [***want to look at diff. materials or use of jfet-type gates to decrease gate leakage without using diode***]. The simulated C-2DFET loaded inverter transfer characteristics are shown in Fig. 5 for a supply voltage of $V_{DD}=0.8 \text{ V}$. The two curves in Fig. 5 represent the inverter characteristics using the simulated $1.0 \times 1.0 \text{ }\mu\text{m}$ p-channel device from Fig. 2 ($V_t=1.0 \text{ V}$)

and the same p-channel device except with the threshold voltage optimized (to $V_t=0.2$ V) for maximum noise margin. The n-channel device is based on an experimental 0.4×0.8 μm device reported in [3] which has approximately the same peak current levels as the simulated p-channel device. The optimized simulation predicts excellent low power switching behavior including a noise margin of 0.22 V and voltage gain of 10 at a supply voltage of $V_{DD}=0.8$ V.

By integrating several inverters in series, we have simulated ring oscillator performance in order to evaluate the potential for future high speed, low power applications. In Fig. 6, we show the transient simulation of an 11-stage ring oscillator using complementary 2-D MESFET logic with a 0.8 V supply voltage. The gate switching delay was 39.5 ps and the power consumption was $0.75 \mu\text{W}$ per gate. By varying the parameters of the individual FETs (e.g. threshold voltages, channel length), we observed small and offsetting changes in the delay and power, as expected. In each case, the resulting power-delay product was less than 0.1 fJ. This result, which is plotted in Fig. 7, represents a very substantial reduction in the power-delay product compared to the state-of-the-art in competing transistor technologies. The main reasons for such a reduction in the power-delay product are the elimination of the narrow channel effect and the use of the heterodimensional 3-d/2-d Schottky contact which has a lower capacitance than the equivalent parallel plate device. Most important, the stand-by power dissipation (of inactive gates) is reduced using the complementary approach by more than a factor of 6 as compared with the DCFL approach, resulting in a significant reduction in total power consumption.

Finally, we simulated a C-2DFET NOR gate using the two-input AIM-Spice model based on the wiring diagram of Fig. 4 (right). The result is shown in Fig. 8. The inputs are 10 μs voltage pulses. As evident in the figure, the output is high only when both inputs are low; thus, the logic element is a NOR gate. NAND gate operation is also possible with the correct choice of threshold voltages in the n-channel and p-channel devices. Three-input logic elements may also be possible by using the dual-input capabilities of both the n-channel and p-channel devices. So, in addition to operating at a very low power-delay product, the dual-gate aspect of the 2-D MESFET allows greater functionality using fewer gates than other digital technologies

Task 4: Manufacturability and Technology Insertion Issues

Several issues concerning the manufacturability of the C-2DFET technology have been explored. First, a literature search of existing complementary FET technologies was performed to compare the competing low power transistor technologies and to serve as a basis on which to evaluate the C-2DFET results we obtained [4-7]. The results of this search (Fig. 7) indicate the C-2DFET technology has a significant advantage in gate power-delay product, especially on the power side of the equation. Second, we considered the feasibility of manufacturing both n-channel and p-channel devices side-by-side using ion implantation and concluded that the approach is certainly realistic and may even lead

to smaller transistor spacing (between n- and p-channel devices) and therefore to higher integration densities. This results primarily from the much smaller (e.g. sub-micron) channel dimensions possible using the C-2DFET approach and the power dissipation is much less a problem compared with conventional CHFET technologies. Third, we evaluated the entire fabrication process and concluded that C-2DFET circuits can be manufactured using entirely conventional process technologies. This fact will enable C-2DFET circuit manufacturing once the device technology is optimized. Finally, we discussed the prospects for low power electronics with several experts in the field [8] and conclude that the market for such technologies is growing rapidly due to the strong demand for wireless communications devices. We believe that the C-2DFET technology can play an important role in future low power electronics for both consumer and critical military electronics needs.

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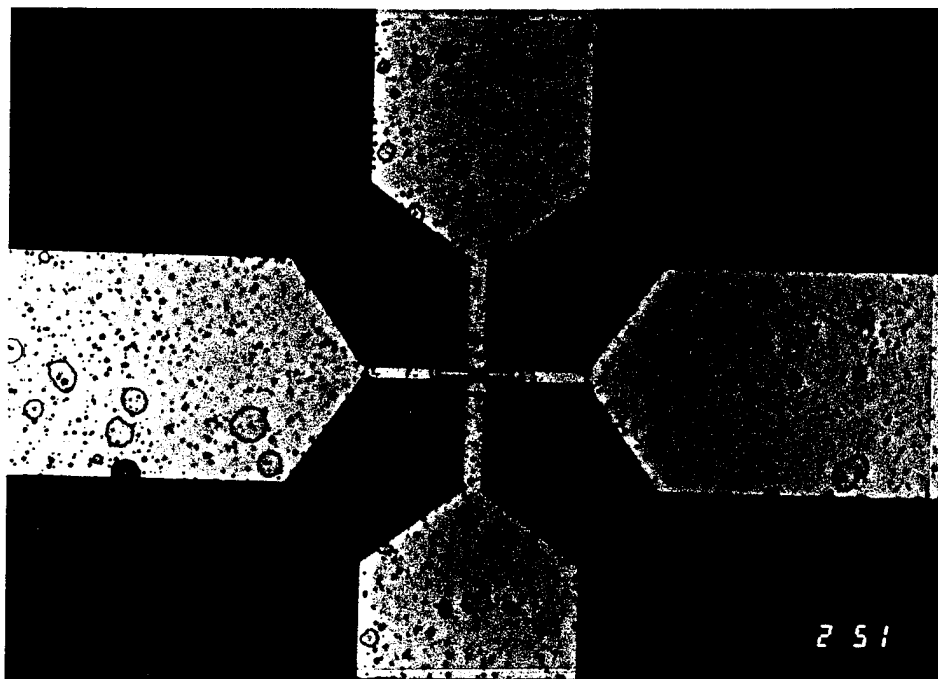


Fig 1. Photograph of a prototype p-channel 2-D MESFET.

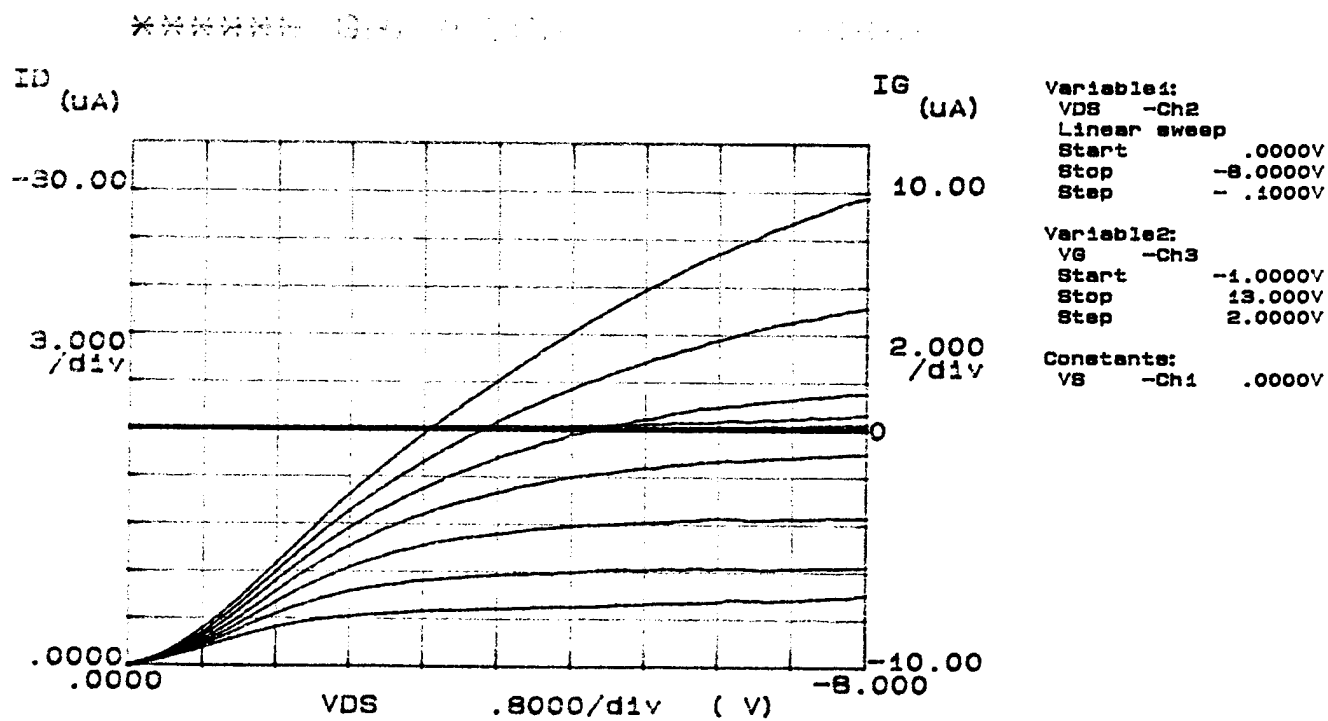


Fig 2. I_D - V_{DS} characteristics of prototype p-channel 2-D MESFET at 300K.

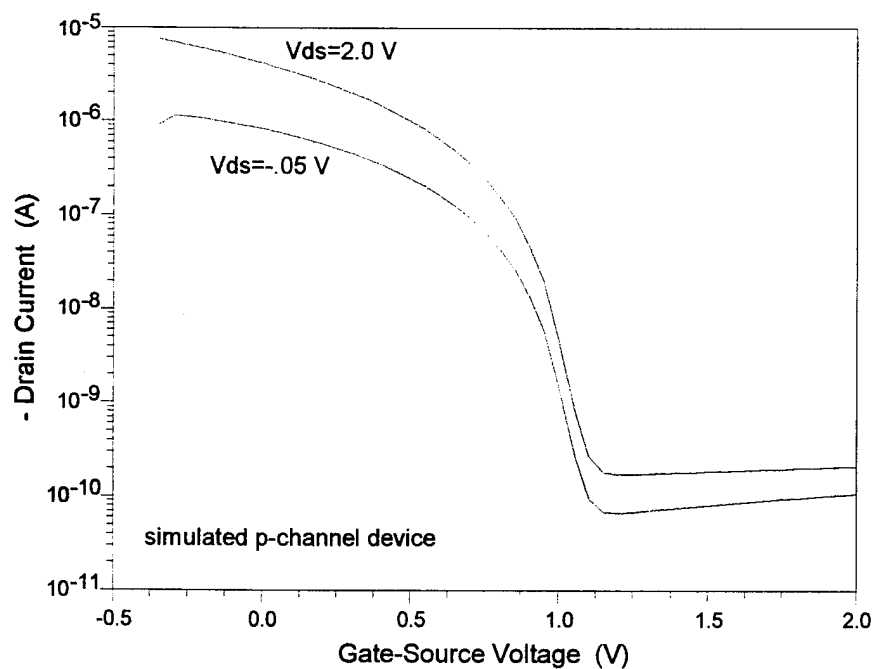
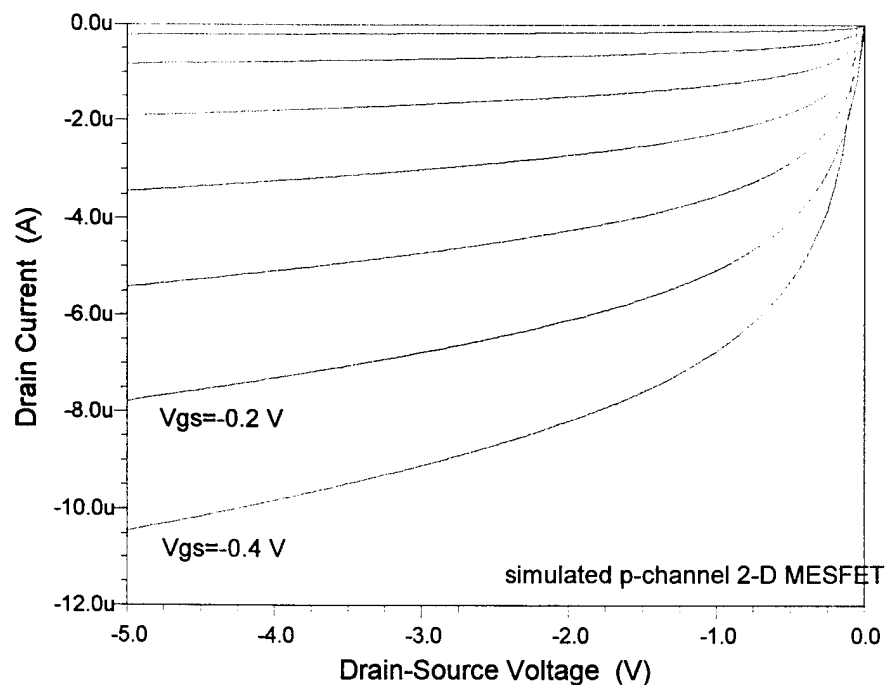


Fig. 3. Simulated p-channel 2-D MESFET. Simulation is based on prototype device PQ2A2C, except series resistance has been optimized to $10 \text{ k}\Omega$ and channel dimensions scaled to $W=L=1.0 \text{ }\mu\text{m}$ (thereby scaling V_t to 1.0 V). All other extracted device parameters are the same as for the prototype device.

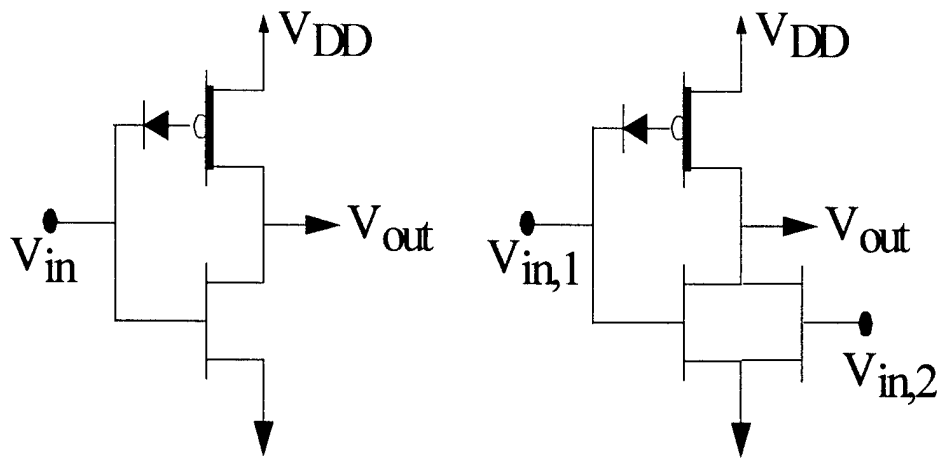


Fig. 4. Wiring diagrams of a complementary 2-D MESFET inverter (left) and NOR gate (right).

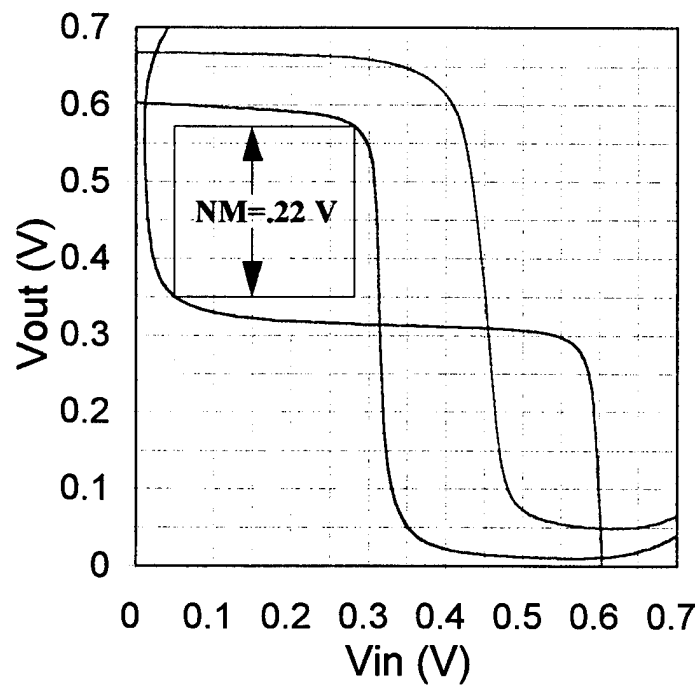


Fig. 5. Simulated inverter characteristics of C-2DFET using $V_{DD}=0.8$ V. Top curve uses $V_{tp}=1.0$ V, bottom curve is optimized for 0.6 V logic and uses $V_{tp}=0.2$ V.

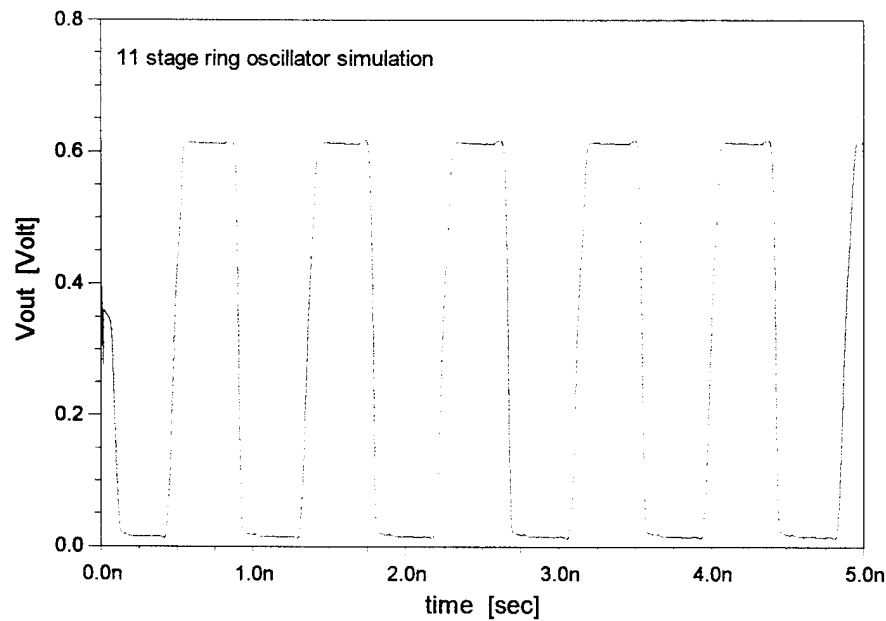


Fig. 6. Complementary 2-D MESFET DC ring oscillator simulation (11-stage) showing a gate delay of 39.5 ps and power of 0.75 μ W.

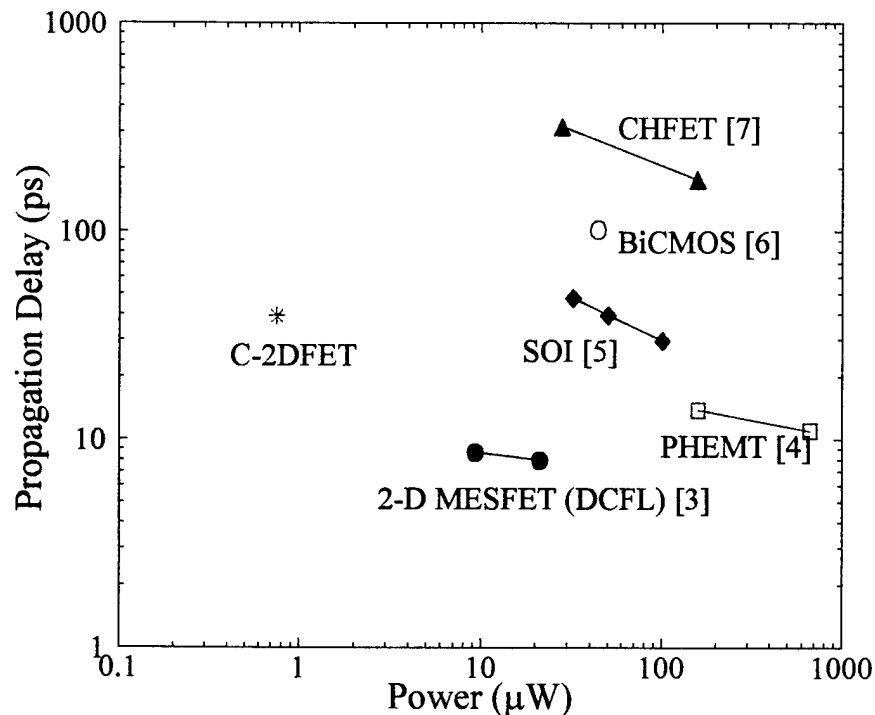


Fig. 7. Ring oscillator gate delay versus power of various low power electronics technologies. The simulated C-2DFET ring oscillator $\tau \cdot \Delta t$ product is much lower due to lower junction capacitance and superior low power properties in sub-micron width devices.

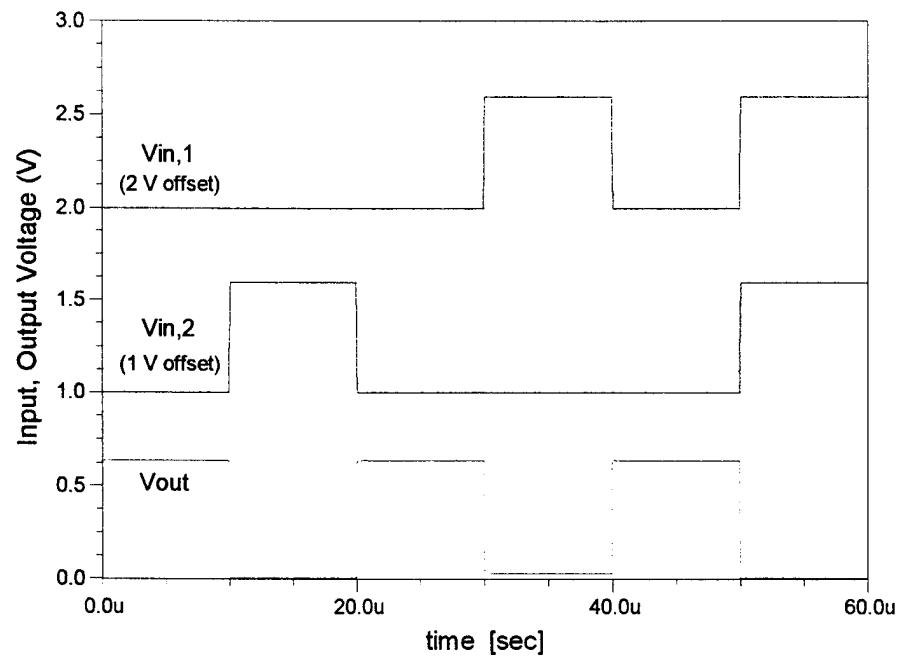


Fig. 8. Simulated transient response of two-input C-2DFET inverter illustrating NOR function (see Fig. 3).

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